## Fp Ccd Camera System (CREOTECH)

### CCD Camera main building blocks

Camera assembly is critical part of the NEOSTEL project, it consists of the following sub-blocks:

* Mechanical Case
* Cooling system including cooling rack
* Shutter mechanism
* BI CCD and Analog Front End (AFE)
* Sensor controller and communication interface
* Camera Housekeeping and control workstation

The scheme of the NEOSTEL Camera is presented on the Fig. 7-5.

Neostel_camera.emf

Figure ‑: CCD Camera Architecture system

**Mechanical case**

Based on the preliminary design studies performed by Creotech, the following design lines will be applied. The external envelope of the camera interface will measure less then 250 mm in diameter. Cylindrical shape of the enclosure is the aim but rectangular shape is also possible. Cylindrical construction of the sensor chamber is recommended due to vacuum seal constraints. Camera will have flange interface to mounting. Window material will be silica glass with broadband AR coating. Position of CCD sensor surface will depend on the window thickness. The construction will be based on already proven K20/K30 cameras (Fig. 7-5.1) – liquid cooling will be used instead of heat sink and shutter will be installed outside of the chamber. Design will be compliant to the worst case environment conditions on the site where the camera will be installed.

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*Fig. 7-5.1: K2/K20/K30 cameras structure*

### Cooling system including cooling rack

The CCD sensor operating temperature is -50°C. To achieve this value, a vacuum chamber will be used. Filling the chamber with a noble gas will be considered. CCD sensor liquid cooling will be used, most probably with water-glycol. Fans are not allowed in order to minimize the vibration level. Double or triple stage TEC modules will be used. Problem of heating CCD sensor (chimney effect) will be minimized by sensor power management. This approach was verified in K20/K30 cameras and simply relies on reducing the CCD outputs stage voltage during the charge integration period.

Project also includes fluid control rack for camera cooling. We will use custom-of- the-shelf, rack mount chiller (Fig. 4).

The chiller is equipped with temperature and flow sensors and its operation is managed by the camera software directly using the serial port. Moreover, independent temperature sensors will be implemented in each camera on the coolant inlet and outlet. Both sensors have hardware alarm output that will be wired directly to the power management system of the camera to shut down the TEC supply without need of software intervention. This is second level of thermal protection. First level is ensured by the management software.

The TEC supply will be controlled locally by each camera power management block and temperature will be stabilized using a PID loop. PT-1000 or similar temperature sensor will be installed just at the CCD sensor enclosure to minimize the temperature stabilization loop time response.

Temperature control of the sensor is critical for long exposure times. We estimate the stability of the temperature to be below 0.01 degrees. Sensor temperature is logged and added to each image FITS header. CCD temperature measurement accuracy is about 0.1 degrees.

Thermal energy from the TEC module will be received by a water block. Creotech has already built a series of cameras equipped with this form of cooling (Fig. 7-5.2, Fig. 7-5.3, Fig. 7-5.4).

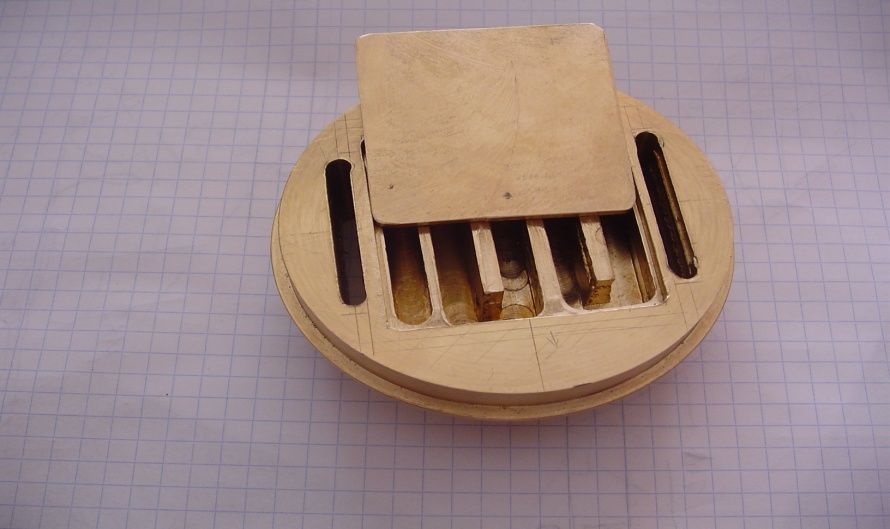
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Fig.7-5.2: Water block used in K10 cameras; Fig.7-5.3: K10 cameras with liquid cooling

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*Fig. 7-5.4: 19" rack mount 725W chiller*

### Shutter mechanism

A custom shutter for CCD sensor will be designed. For the NEO application, exposition times are in the range from 10 sec to 300 sec with accuracy of +-5 ms. Non-uniformity of CCD sensor pixel exposition will be less then 5ms for this application. Shutter life time of is at least 10^6 cycles. Shutter time synchronization error will be less then 100 μs. PTP protocol will be used, UTC time for blades opening and closing will be recorded. PTP time will be delivered directly to the FPGA registers and used to time-stamp the shutter operation entirely in hardware to minimize the latency caused by the software.

There will be an internal and external (via RS485 interface) shutter trigger. Acoustical noise will be taken in the consideration while designing the shutter. For the SST application timing specifications are more stringent: minimal exposure time is 800 ms, non-uniformity pixel exposition less then 0.5 ms and synchronization time will be less then 0.1 ms. Also, in the SST application it is necessary to keep track of exact time (UTC) of each pixel opening and closing by shutter blades. The NEO specification is the goal for this project, whereas the SST specification will be taken into consideration but is not guaranteed to be achieved.

Creotech developed several shutter topologies.

Historically, the first and the most reliable (proven 10e7 cycles) were based on 2 linear voice-coil motors supported by the motion controller implemented in the FPGA. It works without feedback and relies on mathematical model derived from measured step response of the shutter mechanism (Fig. 7-5.5).

In case of the shutter, an additional high resolution magnetic encoder will be used. Optical encoders are not suitable in this project since they can cause parasitic light that affects the measurement. Our experiments have shown that it is difficult to shield them optically for high integration time.

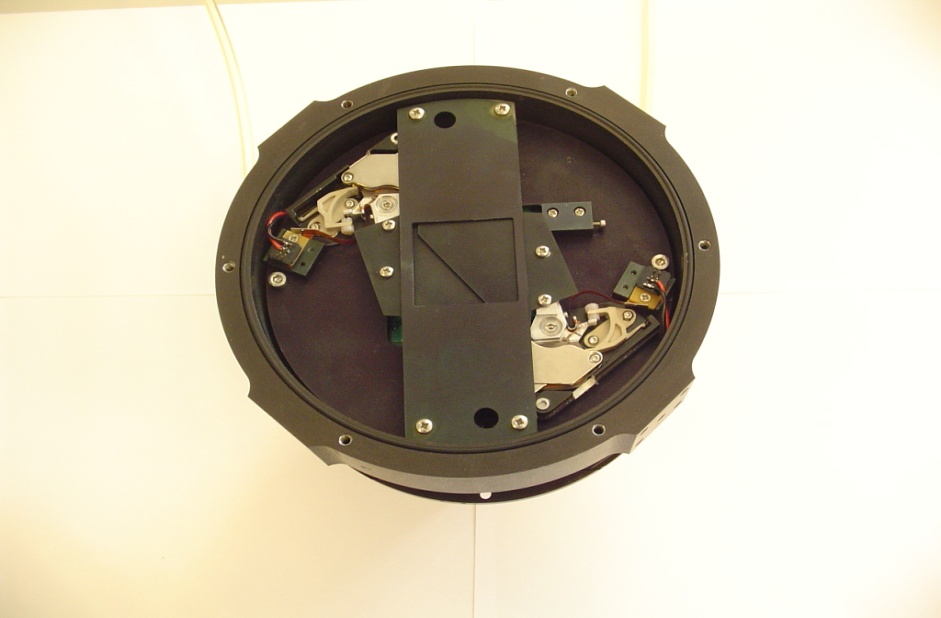
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Fig. 7-5.5: Shutter mechanism used in K2/K20/K30 cameras

We have also developed another shutter mechanism that ensures better control of the integration time precision (Fig. 7-5.6).

In case that existing shutter topologies do not fulfil project requirements, other concepts are considered, i.e. based on LCD technology. Recently it can be observed a continuous progress in this technology.

The final selection of the technology will be undertaken after detailed studies on the shutter mechanism in the course of the NEOSTEL project providing the required parameters: non-uniformity of CCD sensor pixel exposition, shutter life time and shutter time synchronisation error entirely fulfilled for NEO application and the best possible for the SST application.



Fig. 7-5.6: K40 shutter

### BI CCD and Analog Front End (AFE)

Back Illuminated (BI), Full Frame Transfer (FFT) CCD sensor with 4k×4k active pixels will be used for the NEOSTEL camera. MPP (Multi Pinned Phase) option is foreseen for the user to eventually reduce dark current.

It is proposed that the CCD sensor and the low noise preamplifier will be installed inside of the camera vacuum chamber. The sensor assembly will be connected with feed-throughs using flexible PCB. Rigid-flexible PCB technology ensures optimal weight, relevant thermal characteristics and lack of additional connectors between CCD board and flexible cables. This solution improves reliability.

10 electron of read out noise at 2Mhz will be guaranteed by low noise design, fully differential signal chain and dedicated ADC converters working in CDS mode, possibly with oversampling. Dynamic range of the signal is required to be at least 20ke-/e- with a 16bit depth, due to the fact that during long exposures brilliant stars will saturate their corresponding pixels, whereas faint objects with low SNR shall be also detected..

Two approaches will be tested to fulfill the above requirement:

* a standard one with SAR, 18bit ADCs with an additional analogue CDS sampler and
* a digital CDS based on a high speed pipelined, 16bit ADC.

2MHz pixel rate is a boundary where these two acquisition techniques have similar properties. Four readout channels are considered to achieve 2 s readout time.

An AFE (Analog Front End) will be placed partially on the main camera board, but will be covered by additional shield and connected to the CCD sensor using a differential electrical interface to increase noise immunity.

In K2/K20/K30 designs, the AFE was integrated within sensor chamber, but in case of a vacuum design, thermal dissipation will be a problem. In our K40 design, whole analog part was placed on a dedicated AFE board. Optimal placement of noise-critical AFE part still needs to be investigated. An ADC due to number of interconnectivity with the FPGA, will be placed close to the controller board.

Within the vacuum chamber, temperature and humidity sensors will be installed to measure air leaking into the chamber.

### Sensor controller, triggering and communication interface

The camera construction will be based on the recent FPGA technology development. 7-series FPGA from Xilinx will be considered. Particularly suitable for such application is ZYNQ series System on-a Chip that, apart from FPGA, provides 2 fast ARM CPU cores. This enables a compact design, lack of communication bottlenecks and native Linux support for FPGA resources including live reconfiguration mechanisms.

Precise time synchronization of the readout and shutter operation will be ensured by the readout and shutter controllers implemented entirely in hardware, particularly to avoid an image smearing in case the read-out starts before complete closing of the shutter.

A low jitter, of the order of +/-0.3 pix is considered as a target in order to guarantee homogeneity. In order to precisely know the position of the shutter blade(s) during opening and closing a high precision encoder will be considered joined to the PTP timing.

In the proposed solution the shutter can be triggered by the camera on the basis of its operational status (exposing, readout). An external trigger will then synchronize all cameras in order to have coincidence of the cameras operational statuses. Trigger opto-isolation will be provided to avoid ground loops.

Synchronization between cameras will be ensured by a central trigger that will coordinate the different cameras functionalities in order to keep them in temporal coincidence.

Communication interface will be provided by the SFP+ cage (Small Form-factor pluggable Transceiver) Several types of optical or copper transceivers can be installed. Gigabit Ethernet or PCI Express Gen II protocols can be used without hardware modifications.

To enable cooperation between several cameras, Gigabit Ethernet with the TCP protocol will be implemented. This will provide an option for the camera of full autonomy of control and data acquisition. Since each camera will have an independent operating system, it can store directly the measurement data (FITS files) using NFS protocol on the suitable server.

The main power supply converter will be placed at some meters away from the camera (typically 7-8 but can be increased even up to 15 m). 12V or 24V DC supply will be used. The camera will accept DC voltage and convert it internally to several low voltages suitable for the FPGA and the CCD sensor. To conform to EMI requirements, power supply block will be shielded and placed on dedicated module, as it was done in K20/K30/K40 cameras. The voltage and current consumption of critical supply buses as well as critical electronic component temperature will be monitored and stored in log files.

The CCD sensor supply will be based on already proven, programmable unit that enables precise control of all critical bias voltages and clock levels during camera operation. This enables the readout noise optimization, calibration and ageing effects elimination by running autonomous test procedures.

There will be an AUX accessory port for power supply and I2C protocol for auxiliary peripheral devices that may be connected to the camera in the future.

The camera controller board will be very compact; we will base the NEOSTEL Camera design on the K30 camera design for this purpose (Fig. 7-5.7). In the K30 camera the FPGA and ARM processors were separate components, whereas a single, ZynQ series, chip is proposed to be used in the NEOSTEL Camera instead.

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*Fig. 7-5.7: K30 controller and interface board*

Software part of the design consists of several parts:

* Linux operating system running on embedded ARM processors
* PTP daemon implemented partially in the FPGA circuitry and integrated with the network stack,
* HDL code that implements: the CCD readout state machine, the AFE state machine, the shutter controller, a PTP and time-stamping block, memory controller, network connectivity (SFP gigabit interface),
* INDI server that receives commands over Ethernet and translates them into camera actions,
* hardware drivers for sensors and diagnostics, an image sensor, network interface, FPGA internal communication bus.

Substantial part of the software was already proven in K30 design, PTP and gigabit interfaces were also tested in other ZynQ based projects developed by Creotech.

### Camera Housekeeping and control workstation

Management, data storage and housekeeping of several cameras will be provided by a single, rack-mount, x86 CPU-based server running Linux. It will be connected directly with cameras using Gigabit Ethernet fibres and will run acquisition software.

K30 cameras developed by Creotech are using INDI protocol to communicate with the management system. They can also store FITS files directly to the server using the NFS protocol. We plan to keep this architecture in the NEOSTEL Camera design since it has already proven work reliability.

The FITS format is very versatile since it allows storage of several non-typical parameters in its header. It is useful for monitoring purposes since we want to monitor temperature and humidity inside and outside the chamber, vibration level, critical digital voltages and currents, TEC current, CCD voltages, an operational status (exposure, readout, idle, failure, vacuum, etc.). It is proposed that liquid cooling flow will be monitored with two temperature sensors at the input and output pipes of the camera.

Calibration activities: flat fielding, dark fielding, bias subtraction, pointing model update and bad pixels masking will be handled by software, but can be also implemented in the camera firmware when necessary.

### Camera requirements

The camera parameter specification list, provided below, is preliminary (based on research and laboratory tests on previous Creotech cameras) and might be a subject of change in course of future work progress stages or when new requirements or new technology arises.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Parameter** | **Value** | **Remarks** |
| 1 | Resolution | 4096x4096 |  |
| 2 | Pixel size | 15x15 um | or similar |
| 3 | Sensor architecture | Full Frame Transfer., back illuminated |  |
| 4 | Shutter life time | Mechanical, 10e6 cycles |  |
| 5 | Multi Phase Pinning | Yes, user controllable |  |
| 6 | Linearity | <1% | 100e – 95% saturation |
| 7 | Dark current | < 0.1 e-/s/pix |  |
| 8 | Fill factor | 100% |  |
| 9 | Well depth | 150-200ke- |  |
| 10 | Chamber medium | Vacuum | considering filling with a noble gas |
| 11 | Readout noise | 10e- RMS | @2MHz |
| 12 | Dynamic range | 20ke/e | 16 bit depth |
| 13 | Readout time | <2s | 4 channels |
| 14 | Cooling | Liquid, -50oC, glycol-water | considering the 16th channels fluidic loop; the delta high of 5m; chiller pump linearity to avoid micro vibrations |
| 15 | QE | >95% peak, >75% mean |  |
| 16 | Shutter time synchronisation | <100µs, PTP, NTP |  |
| 17 | External shutter input | Yes, RS485 | controlled also internally. Consider a trigger line for the 16th channels |
| 18 | Camera operational temperature | -20 ...+30 C |  |
| 19 | Camera diameter | <200 mm | flange interface diameter =250 mm |
| 20 | Supply | External, DC |  |
| 21 | Communication interface | Gigabit Ethernet or PCI Express over fibre | SFP interface |
| 22 | OS drivers | Ethernet, Linux |  |
| 23 | Camera diagnostics | Temperatures (operational), TEC current, CCD voltages, exposure time, vacuum, camera state (idle, readout, etc), |  |
| 24 | Supply cable length | > 20 meters |  |
| 25 | Window material | Silica Glass with broad band AR coating | 5 mm thick, the position of the CCD surface should be set as a function of the window thickness |
| 26 | AUX accessory port | Yes, I2C, supply |  |
| 27 | Shutter non-uniformity | <0.5 ms | <5 ms NEO; <0,5 ms SST; |
| 28 | File format | FITS |  |

### Engineering approach

Requirements for a high quality astronomical camera impose several technical challenges to be approached with care.

**Quality CCD readout**

The most significant issue to be taken into consideration is a high quality CCD readout. Image readout parameters limits are dictated by a CCD sensor and a camera AFE. The problem however is much more complex than a simple choice of an accurate CCD sensor model and should be addressed in early stages of the camera design. As the readout can be easily degraded by Off-Chip working conditions, to obtain a quality CCD readout for scientific applications the design must enforce excellent working conditions for the CCD chip itself and its close peripherals. Low temperature, low humidity and low noise must be the main driving factors of the camera design. On the other hand such requirements create impractical parameters to achieve for the whole design.

To address this issue we propose a camera with a modular architecture design with the CCD sensor being separated, both spatially and electrically, from the rest of the camera electronics. This can be done by mechanical case being divided into two separate sections (ref. fig. 7-5.1):

* **Isolated (clean) cavity for Detector Module (DM)** where a high purity neutral gas or vacuum (under-pressure) can exist.

The detector module with on-board CCD sensor, analog signal buffer and extensive power supply filtering circuitry are residing in this section only. The CCD analog domain is to be carefully separated electrically from the noisy digital domain of the rest of the camera by buffering and filtering techniques. DM can be cooled via TEC unit (2-stage Peltier) which "moves" the heat to the aluminum block from which the cavity is made. Heat from the aluminum block is further moved outside of camera using liquid cold plate. Signals and power to the DM can be passed from the second section through rigid-flex system connections to the feed-throughs which pass the signal to the camera controller. Cavity is to be sealed by the front plate where shutter mechanism and main window resides. In order to achieve pressure tightness o-rings will be utilized in gaps between metal cavity and front plate, and also to seal main window. Low pressure or clean ambient environment in the cavity can be achieved using two connectors for connecting the air pump.

Creation of pressure tightness has a direct impact on long-term purity (quality) of the gas (vacuum) in the CCD chamber, which in turn influences the minimal temperature to which CCD can be cooled down thus influences the minimal dark current noise.

* **Mounting section with cooling system for electronic modules**

Electronic modules can be mounted on each side of the internal chassis which is fixed to the mechanical case. Modules can be easily removed and replaced for upgrading or maintenance purposes. Thermally active (hot) sides of each module are to be pointed to the inside of the case from where heat is transported out of the camera using the liquid cold plate. The Camera case is closed from the back with a user interface panel where connectors are placed.

Based on experience derived from former projects creating 'smart' mounting system to ease camera assembly/disassembly is crucial for maintenance. In proposed design electronic modules are accessible without removing the detector module, thus eliminating probability of contaminating the CCD chamber and damaging the detector which is very sensitive to ESD and very expensive.

**Electromagnetic interference**

As briefly described in previous problem area, electronic modules have to be mounted in separate section than DM. In previous camera models built for the Pi-of-the-Sky experiment (with K20 and K30) electronic components (other than CCD sensor) resided on a single PCB board. Such approach created occasional problems, especially with EMI of conductive type (despite extensive filtering) due to fast and high current drain peaks involving DC/DC converters, TEC drivers and fast digital electronics, thus creating a noise dense environment compromising power and signal integrity of sensitive components.

In the proposed NEOSTEL camera design we will address this issue by separating modules spatially. Each module (and its respective circuitry) shall be arranged within camera case to maximize the heat transfer to the liquid cold plate, in order to maintain their temperature as low as possible. Furthermore, in the proposed design we plan to divide modules, so each of them will perform an "orthogonal" task. Such approach enables the project team to work in parallel on each module separately and enables assignments of experts in particular electronic fields for specific module design, thus accelerating design progress. Another consequence of task division into different modules is creation of relaxed design constraints for each module - in comparison to one single PCB approach.

An additional cost generated by multiple PCBs for production the trade-off of such approach is estimated to be vast filtering elements (mostly capacitors) to provide good power integrity, and quality connectors (rated for high frequencies) for module interconnect system.

**NEOSTEL Camera modular architecture**

Each proposed module of the camera architecture shall be designed with high level of versatility, rendering modules compatible with wide range of solutions to allow easy and cost-effective future upgrades and expansions when new technologies or tighter requirements emerge. Separate "orthogonal" tasks for each module should be chosen and implemented in order to achieve the state where one module redesign does not imply any need of redesigning the whole camera. A brief description of each module is presented below.

Control and Communication Module (CCM)

The main task of CCM is to enable running high level Linux operating system, thus giving the possibility of being operated and programmed as a typical standard PC computer. This approach makes the camera much easier for further development and use in area of on-line image processing (if needed) or data storage. CCM will enable camera to operate in a real-time acquisition mode (with on-line image processing) and in event driven client-server mode.

Second task of CCM (indirectly ensured by Linux services) is to provide network awareness(www, TCP/IP, INDI), enabling standard remote access services (SSH, FTP, etc) and to provide time synchronization services based on PTP. In addition CCM can be optionally equipped with a GPS in order to provide time synchronization when network will be unavailable.

Third task of CCM (indirectly ensured by Linux drivers) is to provide compatibility with standard interfaces for local operation, image preview and data storage with candidates like: USB, RS232, SD-CARD.

Another task of this module is to work as a CCD and AFE controller. Thanks to embedded FPGA, precisely defined digital waveforms are generated that control the charge movement, signal sampling and shutter operation. CCM should possess an ability to generate user-defined CCD clocking waveforms over wide range of frequencies and with high time resolution.

HDL for given FPGA itself is an additional factor to be taken into consideration in the CCM design. Selection of FPGA shall ensure high enough resources for HDL implementation and additional modifications. At present state it is possible to predict amount of needed resources based on experience from previous camera families.

Analog-Front-End Module (AFEM)

The main task of AFEM is to digitalize analog CCD output signals with ADCs and feed them into CCM. AFEM should be separated from the rest of digital modules and from high current sinking components, giving additional noise and jitter immunity. Sampling clock should be generated (or synthesized) locally with low phase noise for further jitter reduction. Digitalized data should be passed to CCM with as low noise induced into sampling process as possible, thus requiring low voltage output (differential) interfaces and additional digital buffering near each ADC component itself.

This approach (with proper PCB routing provided) should enable conversion of the CCD readout without compromising the S/N ratio over wide band of frequencies and should enable (if desired) a development of so called "Zero Noise CCD" concept based on high oversampling ratio (30-100) and digital filtering techniques (implemented in FPGA on CCM).

Trade-offs to consider in AFEM are involved in selection of ADCs and sampling clock generator circuitry. First factor to consider is a technique of the CCD readout (CDS or oversampling) that will imply required ADCs architecture. Second factor is the number of input channels implying the number of ADCs on AFEM. Third factor is the sampling rate and therefore data throughput to be sent into the CCM. The last factor is a phase noise characteristics of the sampling clock generator (synthesizer) circuitry.

Power Supply and Drivers Module (PSDM)

The main task of PSDM will be to provide power to all other modules of the camera - generated from one single standard 12V or 24V power entry. The main feature of PSDM shall be programmability of all voltages needed by the detector module - power, biases, reset and clocking upper and lower levels. The programmable range must fit within safe region defined by the sensor manufacturer.

Construction of the PSDM must ensure optimum heat transfer to liquid cold plate and proper shielding of the DC/DC converters as well as filtration of all the supplies.

**Long-time reliability**

The NEOSTEL camera reliability shall be achieved in two main areas – mechanical and thermal. Mechanical components (like shutter mechanism) are the most common cause of faults – mechanical wear by friction. Furthermore electrical components exposed to too high temperature not only degrade much faster but also generate more bit errors. Both factors need to be minimized for a long-time proper camera operation.

In mechanical area we propose a dedicated shutter mechanism based on previous experiences gathered during development of four camera families. All our shutter mechanisms are designed to limit friction - their targeted life-time spans beyond 10e6...10e7 cycles. Additional R&D need to be performed to verify if refined design meets NEOSTEL requirements.

For such 60x60 mm sensors we propose development of new shutter based on 4 voice coil actuators which proven its performance in our cameras for the Pi-of-the-Sky experiment. The shutters continuously work since 2008 and exceeded 10e7 cycles long time ago.

### Technical feasibility and development risk

The NEOSTEL camera will be designed to provide a high-end instrumentation for observations in field of astronomical all-sky surveys. Successful implementation will depend upon several stages (and their iterations if necessary):

* Detailed end product specification should be created and accepted for feasible and practical realization.
* Careful components selection has to made by respective module designers considering performance, cost, end product working conditions and assembly reliability.
* The Camera case and cooling system have to assure appropriate working conditions vital to high quality CCD readout.
* The shutter mechanism and cooling solution must guarantee long-time operation.
* Design of respective modules must be driven by required specifications and has to insure that each electronic module is possible to be: manufactured, tested, maintained, reused, upgraded in hardware and software areas.
* The prototype has to be assembled, tested (initially in controlled laboratory conditions) and verified in comparison with system requirements, some of which include: CCD (readout and dark) noise and its histogram, CCD dynamic range, max. fps readout, typical data throughput over TCP/IP network, on-line processing limits and off-line processing limits.
* The camera prototype system has to pass targeted environmental tests.

A camera passing above stated stages can be considered ready for further specific application deployment.

Initial work towards the NEOSTEL camera will include:

* consideration of a cuboid shape camera case with internal holder chassis,
* assembling of various blocks evaluation modules for laboratory tests,
* building and tests of two different shutter mechanisms,
* testing various CCD chips (with range limited to laboratory equipment below 16-output stage CCD sensor).

At present, the Creotech camera team is ready to move into first pass (1'st iteration) of 6'th stage - camera breadboard assembly and module integration. This stage shall provide most answers for NEOSTEL related issues and shall dictate right design decisions.

The camera design team is going to provide extensive probable risks and possible counteractions (risk management and contingency plan) before the start of the system design phase. Project team already identified several risks involved in the technology, design approach and with manufacturing processes and actions to be taken in course of the design process. The risk related issues are covered in the Volume II of the proposal, chapter 11. “Risk Register”..